

# Connecting Hardware Support for PoE std IEEE 802.3bt and Beyond

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## PoE Trends and Requirements

Proliferation of Power over Ethernet (PoE) enabled devices and systems continues to drive the need for higher levels of DC power over structured cabling systems. This is being driven by a rapid increase in the total number of PoE devices deployed with each device requiring more power. Through the iterations of IEEE 802.3af, IEEE 802.3at and now IEEE 802.3bt, the maximum current drawn across the cabling infrastructure has been continuously escalating. Although most PoE systems do not utilize the maximum allowable currents on all four pairs, the proposed application standard (IEEE 802.3bt) specifies that up to 1A per pair can be supplied to the device over the structured wiring system.

Standard	Requirements
IEEE 802.3af	1 current loop over 2 pairs, 15.4W injected, 13.5W delivered (0.35A@37V)
IEEE 802.3at	1 current loop over 2 pairs, 30W injected, 25.5W delivered (0.6A@42.5V)
IEEE 802.3bt	2 current loops over 4 pairs, 100W injected (50W per pair-set), 80W-85W delivered (2 x 1A @ 40V-42.5V)
TIA TSB-184	Category dependent, 600mA given 100 cable bundle orientation, 10°C maximum cable temperature rise on Category 5e
TIA TSB-184-A	1A maximum per pair, smaller cable bundles required, higher cable temperature rise allowed
NFPA 70 (NEC)	Limited Power Supply (LPS), Table 11(B), page 70-725 maximum currents for LPS and 30V-60V max (150/Vmax = 2.5A).
UL 1863, UL 60950	Limited Power Supply (LPS) <100 VA Safety Extra Low Voltage (SELV) < 60V

Table 1: Power Delivery Requirements

Concurrently, the TIA is developing TSB-184-A which describes the steps recommended to support these increasing power requirements. Maximum current levels for a structured cabling system are set based on; copper cross sectional area, de-rating necessary for bundling, maximum cable capacity, the maximum environmental temperature, and the maximum allowable temperature rise in the cable. It has been assumed that connectors do not represent the limiting factor in the system. Table 1 provides a listing of requirements across a number of established standards for supporting power delivery over balanced twisted-pair cabling. This assumption is generally correct. However, improperly designed connectivity may not support the required current without detrimental effects.

In addition to normal UL and NEC safety standards, the next level of verification assures that the connectors can continuously conduct required current levels without overheating. Excessive heating can reduce electrical performance characteristics of connectors. Plus, heat can increase the likelihood of failure in the form of trace severing or de-lamination of the printed circuit board FR4 substrate. New standards allow for power insertion on all four pair combinations. As a result, the maximum expected current through a connector is 1A on each of the four pairs.

The current carrying capacity of connecting hardware is determined by the thickness and width of the current carrying printed circuit board (PCB) traces. Industry design rules suggest that a 0.0015" thick (1oz) trace that is 0.015" wide is capable of handling 0.55A of current with less than 10°C of temperature rise. Hubbell Premise Wiring (Hubbell) connecting hardware products have always been designed to exceed this minimum industry requirement on all current carrying paths. Hubbell conducts power testing to ensure that connectivity exceeds minimum requirements and provides at least a 50% current carrying capacity margin over existing and proposed applications.

## Test Setup and Procedure

Table 2 outlines a series of test cases conducted to qualify Hubbell connectivity. Test cases include increasing current levels up to 1.5A through all pairs at the same time while measuring heat rise on the printed circuit board within the connector. This current level represents a 50% increase over the proposed IEEE 802.3bt specification.

Test Case	Test Current per Pair
1	1.5A <sup>1</sup>
2	1.4A
3	1.0A
4	0.7A

<sup>1</sup>1.5A is 50% more current per pair than maximum current specified in IEEE 802.3bt

Table 2: Summary of Test Cases

## Sample Preparation

Thermocouples are used to measure the maximum temperature rise on each sample under evaluation. The worse case location of each thermocouple is selected based on running a set current level through all pairs and capturing a thermal image as shown in Figure 1. Area denoted in black and violet represent locations where temperatures were the highest. Thermocouples are placed at these locations in order to ensure that a worst case temperature rise is recorded for each test case.

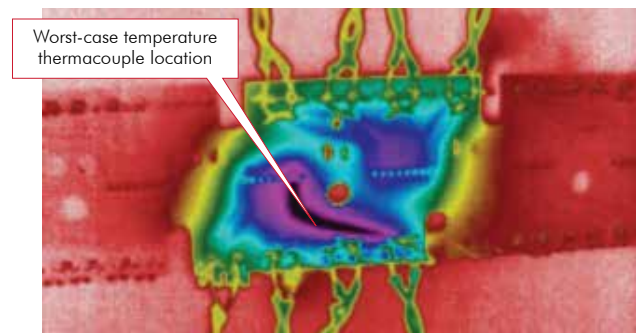


Figure 1: Example of a thermal image used to determine the worst case temperature location

Four samples (or ports) were tested for each product group listed in Table 3. In the case of the patch panels, 4 ports were selected adjacent to each other to capture the worst case heating condition. All 4 samples were tested at the same time placing each in series with a constant current DC power supply. Temperature measurements were collected using a Fluke 2680A data acquisition system with thermocouples connected to a 2680A-PAI precision analog input module.

Category	Outlet, Unshielded	Panel Adapter, Unshielded	Outlet, Shielded
5e	HXJ5e(cc)	HP5e	
6	HXJ6(cc)	HP6	
6A	HJ6A(cc)	HP6A	SJ6A(cc)

Table 3: Product Group Test Matrix

For each test case, samples were energized a minimum of three hours allowing temperatures to stabilize and reach a steady state level for each current. Temperature readings were continuously sampled using data acquisition software. Measurements were recorded for at least a three hour time window into the steady state period. Figure 2 shows a typical thermocouple temperature profile for Test Case 4 running at a current level of 0.7A. All analysis was based on measurements collected within the designated measurement window.

## Results

Summary graphs showing data for each sample tested are provided below. Overall worse case temperature rise and maximum recorded temperature for each product group is shown in Figures 3 and 4, respectively.

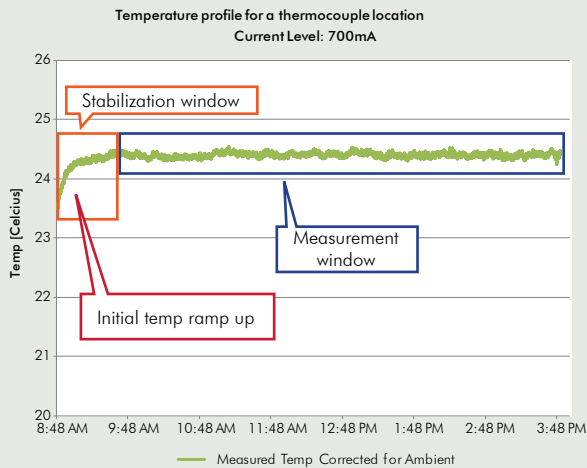


Figure 2: Typical Temperature Profile

For temperature rise calculations, the maximum value taken from data recorded in the measurement window (ref Figure 2) was used in the calculation, ensuring a worst case result. Computed temperature rise for all samples are less than 7°C for the worst case product group. The maximum recorded temperature obtained was 30.3°C. This is well below the delamination temperature of the copper clad FR-4 material used in the PCB which is rated at 140°C.

The maximum temperature rise 7°C is measurably lower than the design target of 10°C. It is also far below any temperature rise limit given in UL 60950. While UL 60950 does not pertain directly to this application, its most stringent temperature rise limit is 30°C and applies to metal parts that are “continuously held in normal use.”

## Conclusion

Qualification results illustrate that Hubbell connectivity is fully capable of handling current levels that exceed the proposed PoE specifications without, any substantial increase in temperature or failure.

The majority of the industry performs testing that is required for mechanical specifications and some safety requirements such as UL1863 and IEC 60603-7-7. Hubbell connectors are designed to exceed these standards and are UL Listed. Even though those standards guarantee safety conditions, they may not indicate whether the hardware is designed to operate under continuous current and voltage conditions. Hubbell performed the current capacity qualification under extreme DTE conditions to ensure support for any established and future PoE applications.

Maximum Temperature Rise

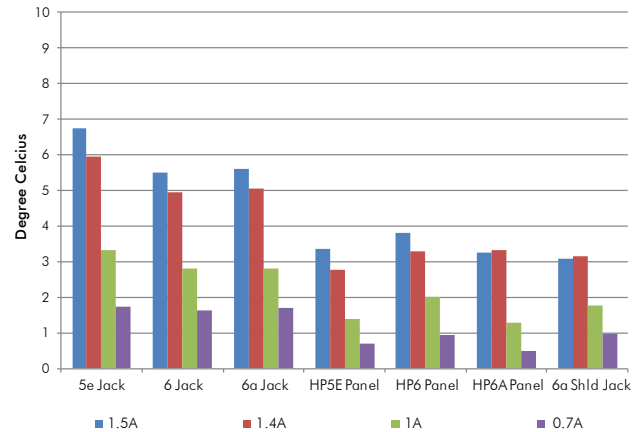


Figure 3: Temperature Rise Graph

Maximum Recorded Temperature

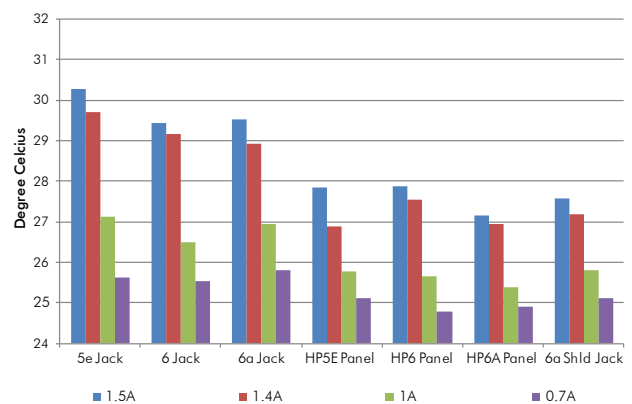


Figure 4: Maximum Temperature Graph

The Hubbell connector design philosophy is to exceed all standards and anticipate future applications for connecting hardware. As a result, the details of design, such as material choices, trace and contact routing and other proprietary design techniques have been optimized with the goal of supporting emerging power delivery requirements. In particular, the PCB trace dimensions and separation are enhanced to provide maximum heat dissipation for reliable, safe, and continuous long term operation.